Please add new claims 8 and 9 follows:

8. (New) The input circuit of Claim 4, wherein the delay means defines the delay time such that an edge of the clock signal, on which the data signal is intended to be latched and which is included within a transition interval of the data signal, is delayed to a point in time after the transition interval of the data signal is over.

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9. (New) The input circuit of claim 4, wherein the first delay circuit defines the delay time based on the result of comparison performed by the comparator and a setup time for correctly latching the data signal, and the second delay circuit defines the delay time based on the result of comparison performed by the comparator and the setup time for correctly latching the data signal.

REMARKS

I. Introduction

In response to the pending Office Action, Applicants have amended Fig. 4 so as to address the objection thereto set forth in paragraph 3 of the Office Action. In addition, claims 3 and 4 have been rewritten in independent format including all of the limitations of original claim 1. Claim 2 has been amended to depend from claim 3. Claim 5 has been amended to address the rejection thereof under 35 U.S.C. § 112, second paragraph. In addition, new claims 8 and 9 have been added. New claim 8 corresponds to original claim 2, and is dependent on claim 4. New claim 9 tracks

original claim 5, and is dependent on claim 4. No new matter has been added.

Applicants acknowledge with appreciation the indication of allowable subject matter recited by claims 3 and 4. For the reasons set forth below, it is respectfully submitted that all pending claims are in condition for allowance.

II. The Rejection Of Claim 5 Under 35 U.S.C. § 112

Claim 5 was rejected under 35 U.S.C. § 112, second paragraph, for failing to clarify which of the delay circuits set forth in claim 4 the subject matter recited by claim 5 pertained to. In response, Applicants have amended claim 5 such that it only depends on claim 3. In addition, new claim 9 has been added, which expressly references both of the first delay circuit and the second delay circuit recited by claim 4. In view of the foregoing amendments, it is respectfully submitted that the rejection of claim 5 has been overcome.

III. The Rejection Of The Claims In View of Suzuki

Claims 1 and 2 were rejected under 35 U.S.C. § 102 as being anticipated by USP No. 5,952,857 to Suzuki. In addition, claims 3-5 were indicated to recite patentable subject matter for the reasons set forth in paragraph 10 of the Office Action.

In response, Applicants have amended claims 3 and 4 to be in independent format. As amended, both claims 3 and 4 incorporate the limitations set forth in original claim 1. In view of the comments set forth in paragraph 10 of the Office Action, which

states that the indication of allowance of the claims is based on the subject matter set forth in claim 3 and 4, it is respectfully submitted that, as amended, claims 3 and 4 are now in condition for allowance. Specifically, as both claims 3 and 4 recite a comparator for comparing the edge of the clock signal, on which the data is intended to be latched, to at least one of the leading and trailing edges of the data signal, and at a minimum, Suzuki does not disclose this element as acknowledged in the Office Action, Suzuki does not anticipate amended claims 3 and 4.

As such, it is respectfully submitted that claims 3 and 4, and all claims dependent thereon, are patentable over Suzuki

IV. Request For Notice Of Allowance

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

Respectfully submitted,

McDERMOTT, WILL & EMERY

Date: 1/3/03

By: _____

Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W. , Suite 1200
Washington, D.C. 20005-3096
Telephone: 202-756-8000
Facsimile: 202-756-8087
WDC99 635050-1.043889.0861

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claims 1, 6 and 7, have been cancelled without prejudice.

Claims 2-5 have been amended and new claims 8 and 9 have been added as follows:

2. (Amended) The input circuit of Claim [1] 3, wherein the delay means defines the delay time such that an edge of the clock signal, on which the data signal is intended to be latched and which is included within a transition interval of the data signal, is delayed to a point in time after the transition interval of the data signal is over.

3. (Amended) [The] An input circuit [of Claim 2] comprising:

delay means for defining a delay time for at least one logical state of a data signal and thereby delaying a clock signal for the delay time defined; and

a holding circuit for holding the data signal responsive to the delayed clock signal;

wherein the delay means comprises:

a comparator for comparing the edge of the clock signal, on which the data signal is intended to be latched, to at least one of leading and trailing edges of the data signal; and

a delay circuit for defining the delay time based on a result of comparison performed by the comparator.

4. (Amended) [The] An input circuit [of Claim 2] comprising:

delay means for defining a delay time for at least one logical state of a data signal and thereby delaying a clock signal for the delay time defined; and

a holding circuit for holding the data signal responsive to the delayed clock signal;

wherein the delay means comprises:

a comparator for comparing the edge of the clock signal, on which the data signal is intended to be latched, to leading and trailing edges of the data signal;

a first delay circuit for defining the delay time for a logically high state of the data signal based on a result of comparison, performed by the comparator, between one of the leading edges of the data signal and the edge of the clock signal;

a second delay circuit for defining the delay time for a logically low state of the data signal based on a result of comparison, performed by the comparator, between one of the trailing edges of the data signal and the edge of the clock signal; and

a selector for selecting the delay time defined by the first delay circuit when the data signal is in the logically high state or the delay time defined by the second delay circuit when the data signal is in the logically low state.

5. (Amended) The input circuit of Claim 3 [or 4], wherein the delay circuit defines the delay time based on the result of comparison performed by the comparator

and a setup time for correctly latching the data signal.

Please add new claims 8 and 9 follows:

8. (New) The input circuit of Claim 4, wherein the delay means defines the delay time such that an edge of the clock signal, on which the data signal is intended to be latched and which is included within a transition interval of the data signal, is delayed to a point in time after the transition interval of the data signal is over.

9. (New) The input circuit of claim 4, wherein the first delay circuit defines the delay time based on the result of comparison performed by the comparator and a setup time for correctly latching the data signal, and the second delay circuit defines the delay time based on the result of comparison performed by the comparator and the setup time for correctly latching the data signal.